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Original Article

A High-Resolution Single-Source Three-Phase Switched-Capacitor Inverter with High Voltage Gain

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Abstract: *A novel three-phase switched-capacitor (SC) topology is proposed in this paper. A seven-level line-to-line output voltage waveform is generated by the fundamental structure of the proposed topology, which includes eight switches and two capacitors, per phase leg. The proposed topology has several main features, including increased boost capabilities, lower voltage stresses, and a minimum number of device counts. Switched capacitors also have built-in capacitor voltage balancing, eliminating the need for a separate balancing circuit. The modulation technique is used to keep the capacitors self-balanced for all values of the modulation index. In this paper circuit description, mode of operation, and modulation strategy is discussed thoroughly. Lastly, simulation results are provided to validate the feasibility of the proposed inverter.*

Keywords: *Multilevel inverter, switched-capacitor, voltage boosting, self-balancing.*

I. INTRODUCTION

Multilevel inverters (MLIs) have been widely studied for low, medium, and high voltage applications [1-2]. The superior features of the MLIs are low voltage stress on the switches, low total harmonic distortion, low dv/dt, fewer requirements of the filter circuit, and high modularity [3]. Several renewable energy sources, such as solar arrays, wind turbines, and fuel cells, are being used to create electrical power. However, the amount of electricity accessible from these sources is restricted [4]. As a result, it will fail to fulfill the power quality requirements of a wide range of applications (such as electric vehicles, fuel cell vehicles, grid connections, and industrial applications). As a result, converting the alternating voltage to a greater voltage is required. To boost the AC voltage, a front-end dc-dc converter with a normal MLI or a load-end transformer is a common solution. [5-6].

The conventional multilevel inverter comprises three basic structures, which are cascaded H-bridge (CHB), flying capacitor (FC), and neutral point clamped (NPC) inverter. Each topology has advantages and disadvantages. For instance, the conventional CHB has a modularity feature. The primary drawback is that separate DC sources are required. Similarly, with NPC and FC topologies, the requirement for clamping diodes and capacitors, as well as the resulting voltage balance concerns, provide a challenge. Traditional inverters' uses are limited due to their unfavorable characteristics. The study has focused on a new strategy of SC-based MLIs that can overcome the disadvantages of conventional inverters. The switched capacitor MLIs can boost voltage, self-balance the capacitor's voltage, and effectively extend the number of output voltage levels due to their flexibility. The topologies shown in [6-7] are based on the SC idea and have modularity properties. However, the high voltage stress on the semiconductor switches limits these topologies, rendering them unsuitable for high voltage applications.

Topology [8] shows how a single unit of its basic cell may create a waveform with seven levels of output voltage. While the design contains a symmetrical voltage source, the architecture is more costly and less attractive due to the need for multiple sources and polarity creation through an H-bridge. The topology described in [12-14] employs a greater number of switching components while achieving the lowest gain. Another seven-level approach [16] uses extra switching components and yields less than unity gain. Topology [17] generates seven stages with a voltage boosting capability of three times the input voltage source, but it has the drawback of placing the switches under high voltage stress. In the topologies described in [9-11],[15], is incapable of boosting voltage. according to the study discussed above, most topologies have several drawbacks, including more switching components per level, more voltage stress on the switches, poorer voltage gain, and a lack of boosting capabilities. This encourages the development of a new topology that has the following distinct characteristics: 1. It generates a 7-level line-to-line output voltage waveform. 2. Voltage boost capabilities, i.e., a gain of three. 3. Capacitors'

inherent voltage balancing capabilities. 4. Fewer device counts. 5. Requires just one power source and lower voltage stress on power switches.

II. PROPOSED TOPOLOGY

A. Circuit description

Fig.1 shows the schematic diagram of the proposed three-phase switched capacitor topology. The proposed topology is a three-phase circuit, wherein each phase leg is composed of eight power switches SXi (i = 1, 2...,8) and two capacitors ($CX1$ and $CX2$), where X ∈ phase (a, b, c). It comprises of single voltage source only. This voltage source can receive power from any renewable energy source or battery.

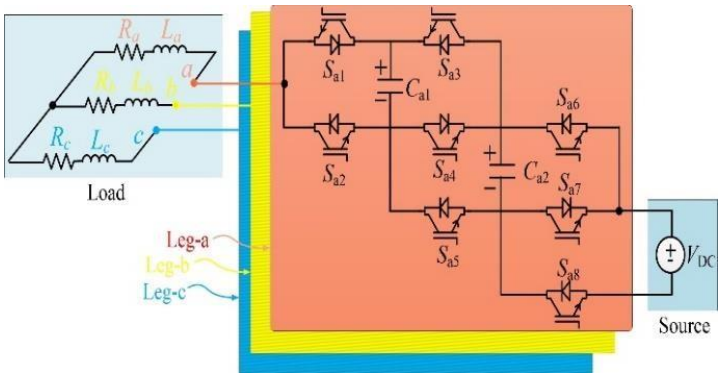


Figure 1: Schematic Diagram of the Proposed Three-Phase Switched Capacitor Topology

When considering the pole voltage VXo(t), the proposed topology can generate four levels i.e., 0, $+VDC$,$+2VDC$,$+3VDC$. Whereas, when considering the line-to-line voltage, the proposed topology can synthesize a seven-level waveform across the load terminals i.e., 0, $\pm1VDC$, $\pm2VDC$, $\pm3VDC$. For a better understanding of the analysis, consider a singlephase leg (a) because the proposed topology possesses symmetricity in all three phases. Table I summarises the valid switching states, where the numbers '1' and '0' denote the ON and OFF states of the switches, respectively.

B. Modes of operation for the pole voltage of leg 'a':

The operating concept of pole voltage (Vao) for the 'a' leg is explained in this section, and a similar analysis can be performed for the other two legs. Capacitor charging path is shown by 'green' and current path by 'red' dotted line in Fig.2. The following modes can be used to describe the whole operating principle of the proposed topology:

State 1: $\boldsymbol{Vao(t)}$ = $\mathbf{0}$ As shown in Fig. 2a the zero-voltage state across the load is obtained by turning ON switches S2a, S3a, S5a, S6a, and S8a and turning OFF S1a, S4a, and S7a. As a result, the capacitors C1a, and C2a are in parallel with the DC source, and hence C1a and C2a get charged to voltage VDC. Therefore, the output voltage ((t)) is 0.

State 2: $\boldsymbol{Vao(t)}$ = $\boldsymbol{VDC}$ This state is obtained by turning ON switches S1a, S3a, S5a, S6a, and S8a and turning OFF S2a,S4a, and S7a as shown in Fig.2b. As a result, the capacitors C1a, and C2a are in parallel with the DC source, and hence C1a and C2a get charged to voltage VDC. Therefore, the output voltage ((t)) is VDC.

State 3: $\boldsymbol{Vao(t)}$ = $\boldsymbol{2VDC}$ This state is obtained by turning ON switches S1a, S4a, and S6a and turning OFF S2a, S3a, S5a, S7a, and S8a as shown in Fig.2c. As a result, the capacitors C1a get discharged. Therefore, the output voltage ((t)) is $2VDC$.

State 4: $\boldsymbol{Vao(t)}$ = $\boldsymbol{3VDC}$ This state is obtained by turning ON switches S1a, S4a, and S7a and turning OFF S2a, S3a, S5a, S6a, and S8a as shown in Fig.2d. As a result, the capacitors C1a and C2a get discharged. Therefore, the output voltage ((t)) is $3VDC$.

Table 1: Switching Operation for Leg 'a'

State	State of Power Switch (1=ON, 0=OFF)								$V_{ao}(t)$
	S_{a1}	S_{a2}	S_{a3}	S_{a4}	S_{a5}	S_{a6}	S_{a7}	S_{a8}	
1	0	1	1	0	1	1	0	1	0
2	1	0	1	0	1	1	0	1	V_{DC}
3	1	0	0	1	0	1	0	0	$2V_{DC}$
4	1	0	0	1	0	0	1	0	$3V_{DC}$

III. MODULATION SCHEME

In the last decade or so, several modulation strategies have been implemented to generate gating pulses for control purposes. Among them, the most popular strategies are (1) Multicarrier PWM (2) space vector PWM (3) space vector control method (4) selective harmonic elimination method. The first two methods are operated with a high switching frequency and the last two methods operate on a low switching frequency [18-20]. This article employs the multicarrier level shift pulse width modulation (LS-PWM) control approach.

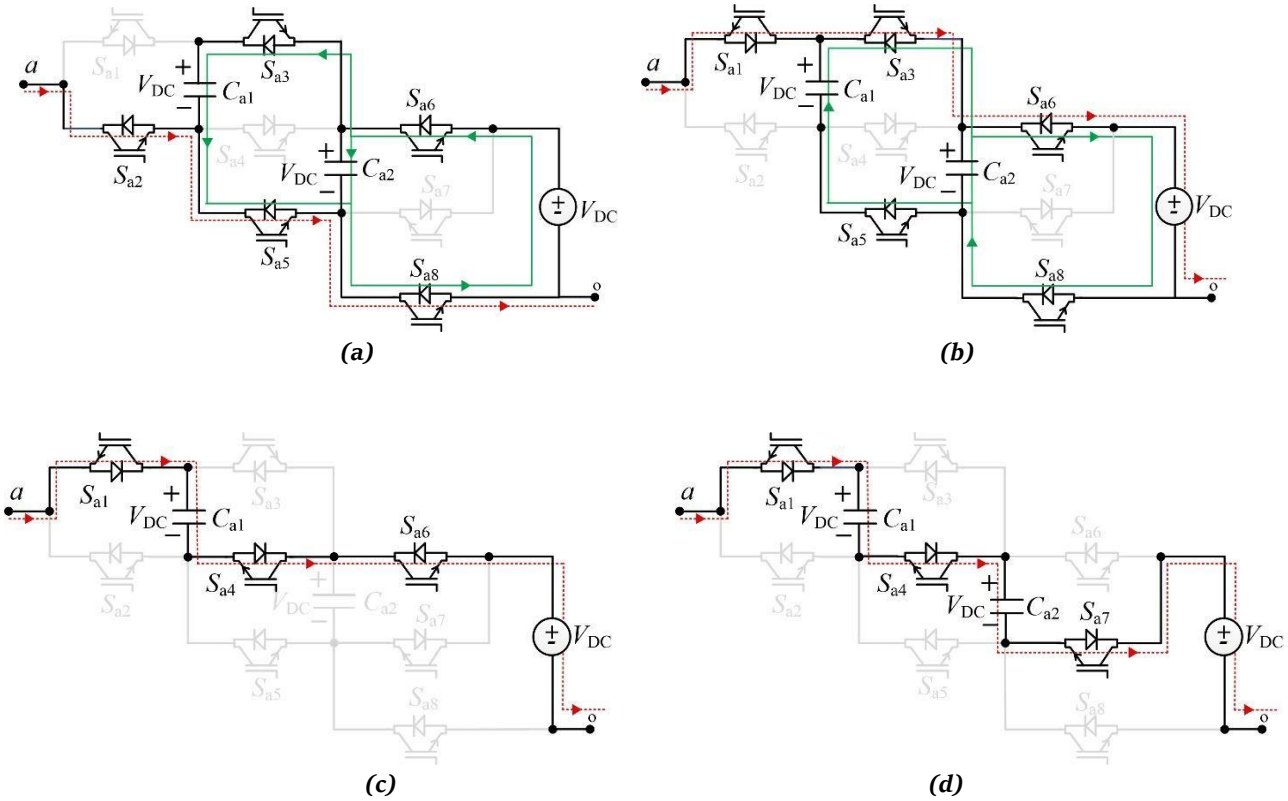


Figure 2: (a-d) Shows the Conducting Paths for Different Modes of Operation for Each Level of Voltage

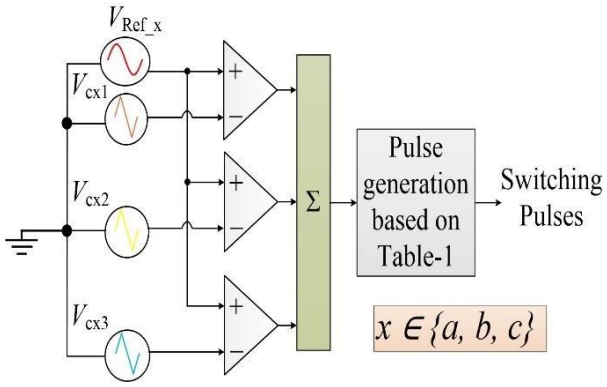


Figure 3: LSPWM Scheme for Phase Leg 'x'

Figure 3: depicts the modulation strategy for the proposed topology. Three carrier signals with constant magnitude and frequency are compared with the modulating signal in this technique. The latter is a reference sinusoidal signal with a frequency equal to 50 Hz. If the reference signal VREF_x is greater than the carrier signals during the comparison, the comparator will output '1', otherwise, it will output 'o'. The comparator will yield 'o' if the reference signal VREF_x is bigger than the carrier signals, otherwise '1'. The comparator output signals are added to produce the aggregated signals. By comparing the aggregated signals to their corresponding constant levels, the switching pulses are obtained. The output of the desired signal is then sent to switches using the pulse generation based on Table 1. However, the suggested topology per phase leg generates only positive pole voltage levels and cannot generate negative voltages. So, the line voltage can be obtained by the following equations:

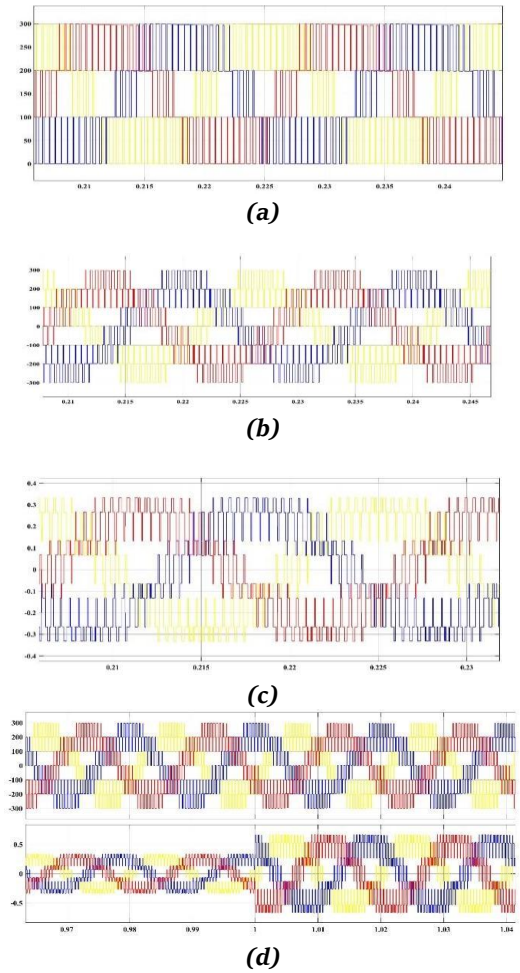
$$= Vao - Vbo \quad (1)$$
$$= Vbo - Vco \quad (2)$$
$$Vca = Vco - Vao \quad (3)$$

VI. SIMULATION RESULTS

A MATLAB/Simulink environment has been used to investigate the proposed topology to verify the theoretical notion. Table 2 represents the circuit parameters used for the Simulink. The simulation results for R load (500Ω) are shown in Fig. 4. The pole voltage is depicted in Fig. 4(a), with four equal step size levels (0, +100V, +200V, +300V). The three-phase line-to-line voltage is presented in Fig. 4(b). It has been observed from the waveform that line voltage has seven levels (0,±100V,±200V, ±300V). The load current is shown in Fig. 4(c). Fig. 4(d) shows the results of output voltage and current for a sudden change in load. When the load is changed from 500Ω to 250 Ω, the output current gets doubled and the output voltage remains the same.

Table 2: Simulation Parameters

Parameter	Specification
Input DC source (V_{DC})	100 V
Output frequency(f)	50 Hz
Carrier frequency	2 kHz
Load (RL, R)	R=50Ω, L=120mH R=500Ω
Modulation index (M)	0.95



(a)

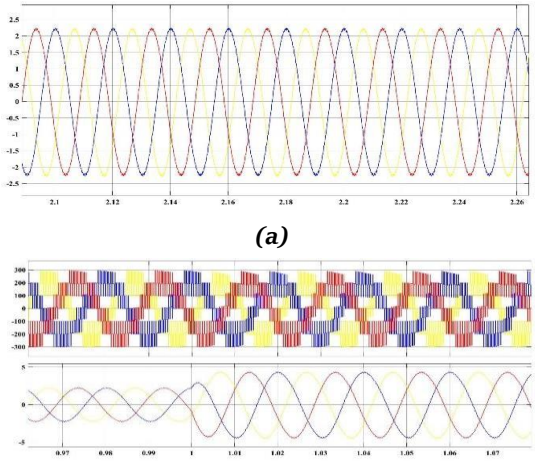
(b)

(c)

(d)

Figure 4: Simulation results for the Three-Phase Proposed Inverter for R-load (a) Pole Voltage (b) Line-to-LineVoltage (c) Output Current (d) Sudden Change in Load

Figure 5 shows the results for R-L load (50Ω,120mH). Figure 5(a) shows the output current with a magnitude of 2.2 A. Sudden change in R-L load is shown in Fig.5(b) where the output current gets doubled by changing load from 50Ω,120mH to 25Ω,60mH. Fig. 6 depicts the Total harmonic distortion (THD) in output current when the load is inductive.



(a)

(b)

Figure 5: Simulation Results for the Three Phase Proposed Inverter for RL-load (a) Output Current (b) Sudden Change in Load

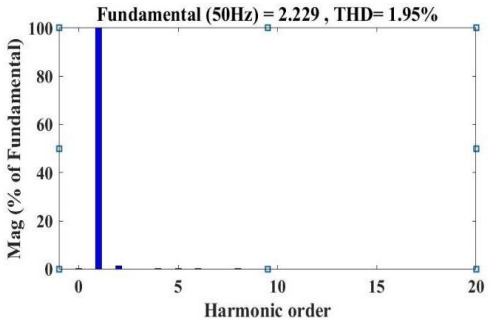


Figure 6: THD of the output current for RL- load

VII. CONCLUSION

This paper introduces a three-phase seven-level inverter based on switching capacitors. The inverter's capacitors rotate between charging and discharging modes, resulting in self-balanced voltages with low voltage ripples. To create a high ac output voltage with several levels, they are coupled in parallel and series alternatively with a dc voltage source. Simulation findings confirmed that the suggested inverter possesses boosting capability and self-balanced capacitor voltages, in contrast to traditional MLIs that have been marketed in medium- and high-voltage applications. As a result, it's better suited to low-voltage applications like EV motor drivers and RES grid-connected interfaces. The great efficiency and outstanding performance under dynamic loads are further demonstrated by simulation findings.

Interest Conflicts

The authors declare that there is no conflict of interest concerning the publishing of this paper.

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